NCP1602

Product Preview

Enhanced, High-Efficiency Power Factor Controller

The 6−pin PFC controller NCP1602 is designed to drive PFC boost stages. It is based on an innovative **V**alley **S**ynchronized **F**requency **F**old−back (**VSFF**) method. In this mode, the circuit classically operates in **Cr**itical conduction **M**ode (**CrM**) when $V_{control}$ voltage exceeds a programmable value $V_{ctrl,FF}$. When $V_{control}$ is below this preset level $V_{ctrl,FF}$, the NCP1602 (versions [B**] and [D**]) linearly decays the frequency down to about 30 kHz until $V_{control}$ reaches the SKIP mode threshold. **VSFF** maximizes the efficiency at both nominal and light load. In particular, the stand−by losses are reduced to a minimum. Like in **FCCrM** controllers, internal circuitry allows near−unity power factor even when the switching frequency is reduced. Housed in a TSOP6 package, the circuit also incorporates the features necessary for robust and compact PFC stages, with few external components.

General Features

- Near−Unity Power Factor
- Two−Level Boost Follower Line Level Dependent (disabled by default)
- Critical Conduction Mode (CrM)
- Valley Synchronized Frequency *F*old−back (VSFF): Low Frequency Operation is Forced at Low Current Levels (9 pre−programmed settings).
- Works With or Without a Transformer w/ ZCD Winding (simple inductor)
- On−time Modulation to Maintain a Proper Current Shaping in VSFF Mode
- Skip Mode at Very Low Load Current (versions[B**] and [D**])
- Fast Line / Load Transient Compensation ***(D**ynamic **R**esponse **E**nhancer)*
- Valley Turn−on
- High Drive Capability: −500 mA / +800 mA
- V_{CC} Range: from 9.5 V to 30 V
- Low Start−up Consumption for:
  - [*B*] Version: Low *Vcc* Start−up level (10.5 V)
  - [*A*] Version: High *Vcc* Start−up level (17.0 V)
- Line Range Detection for Reduced Crossover Frequency Spread
- This is a Pb−Free Device

Safety Features

- Thermal Shutdown
- Non−latching, Over−Voltage Protection
- Second Over−Voltage Protection
- Brown−Out Detection
- Soft−Start for Smooth Start−up Operation ([*B*] Version)
- Over Current Limitation
- Disable Protection if the Feedback Pin is Not Connected
- Low Duty−Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring

Typical Applications

- PC Power Supplies
- Lighting Ballasts (LED, Fluorescent)
- Flat TV
- All Off Line Appliances Requiring Power Factor Correction

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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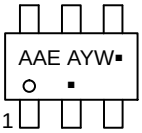
TSOP−6
TBD SUFFIX
CASE 318G

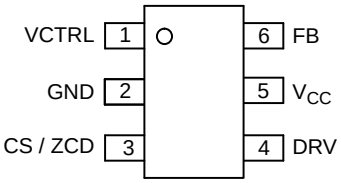
MARKING DIAGRAM



AAE	= Specific Device Code
A	= Assembly Location
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

DEVICE ORDERING INFORMATION

Device Order Number	Package Type	Tape and Reel Size
	TSOP−6 (Pb−Free)	

Several product configurations coded with three letters (L_1,L_2,L_3) marked on the package will be available.

Table 1. NCP1602 1st LETTER CODING OF PRODUCT VERSIONS

L_1	Brown−out Function	Skip Mode Function
A (default)	**NO (default)**	**NO (default)**
B	**NO (default)**	YES (trim)
C	YES (trim)	**NO (default)**
D	YES (trim)	YES (trim)

NOTE: The NCP1602 TSOP6 package is marked NCP1602 – $L_1L_2L_3$

Table 2. NCP1602 2nd LETTER CODING OF PRODUCT VERSIONS

L_2	CrM to DCM V_{CTRL} Threshold (V)	$t_{ON,max,LL}$ (μs)	$t_{ON,max,HL}$(μs)
A	0.816	25	8.33
B	1.026	25	8.33
C	1.296	25	8.33
D	1.132	12.5	4.17
E (default)	1.553	12.5	4.17
F	2.079	12.5	4.17
G	1.459	8.3	2.77
H	2.079	8.3	2.77
I	2.840	8.3	2.77

NOTE: The NCP1602 TSOP6 package is marked NCP1602 – $L_1L_2L_3$

Table 3. NCP1602 3rd LETTER CODING OF PRODUCT VERSIONS

L_3	V_{CC} Startup Level (V)	2−Level Boost Follower Feature
A (default)	**17.0 (default)**	**NO (default)**
B	**17.0 (default)**	YES (trim)
C	10.5	**NO (default)**
D	10.5	YES (trim)

NOTE: The NCP1602 TSOP6 package is marked NCP1602 – $L_1L_2L_3$

The non−trimmed (default) version of the product, marked on the package will be then AEA (L_1=A, L_2=E, L_3=A)
L_1=A meaning NO Brown−out and NO SKIP Mode
L_2=E meaning E version of Frequency Foldback
L_3=A meaning 17V V_{CC} Startup voltage and NO 2−Level Boost Follower Feature

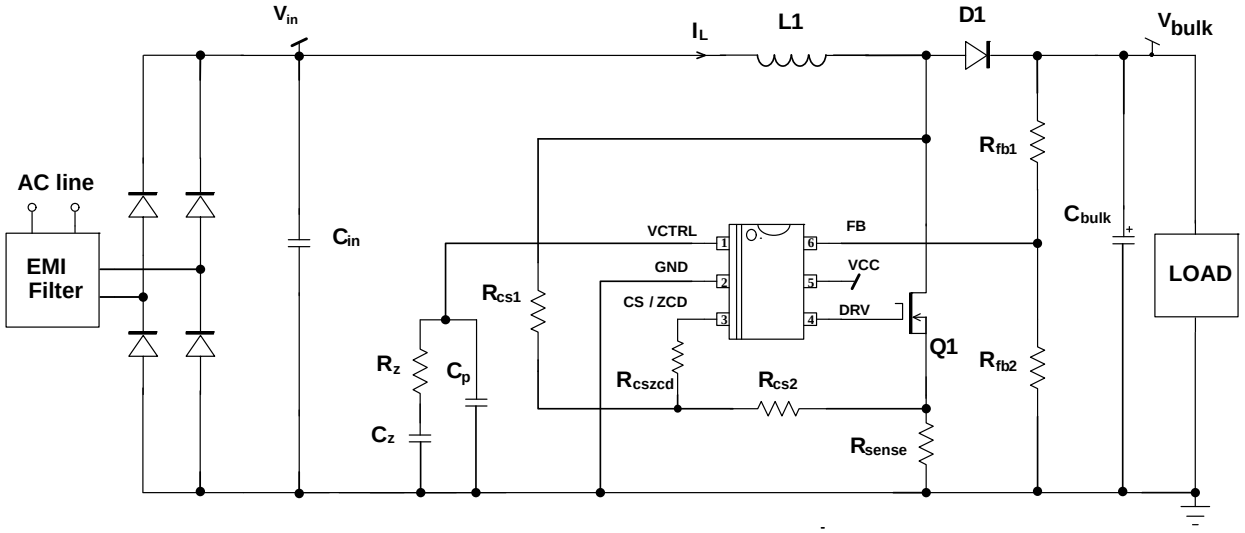


Figure 1. NCP1602 Application Schematic

Table 4. DETAILED PIN DESCRIPTION

Pin Number	Name	Function
1	VCTRL	The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. VCTRL pin is internally pulled down when the circuit is off so that when it starts operation, the power increases slowly to provide a soft−start function. VCTRL pin must not be controlled or pulled down externally.
2	GND	Connect this pin to the PFC stage ground.
3	CS / ZCD	This pin monitors the MOSFET current to limit its maximum current. This pin is the output of a resistor bridge connected between the drain and the source of the power MOSFET. Internal circuitry takes care of extracting V_{in}, V_{out}, I_{ind} and ZCD
4	DRV	The high−current capability of the totem pole gate drive (−0.5/+0.8A) makes it suitable to effectively drive high gate charge power MOSFETs.
5	VCC	This pin is the positive supply of the IC. The circuit starts to operate when VCC exceeds 17.0 V ([**A] & [**B] Versions) or 10.5 V ([**C] & [**D] Versions) and turns off when VCC goes below 9.0 V (typical values). After start−up, the operating range is 9.5 V up to 30 V.
6	FB	This pin receives a portion of the PFC output voltage for the regulation and the Dynamic Response Enhancer (DRE) that drastically speeds−up the loop response when the output voltage drops below 95.5% of the desired output level. FB pin voltage V_{FB} is also the input signal for the (non−latching) Over−Voltage (OVP) and Under−Voltage (UVP) comparators. The UVP comparator prevents operation as long as FB pin voltage is lower than V_{UVPH} internal voltage reference. A SOFTOVP comparator gradually reduces the duty−ratio when FB pin voltage exceeds 105% of V_{REF}. If despite of this, the output voltage still increases, the driver is immediately disabled if the output voltage exceeds 107% of the desired level (fast OVP). A 250−nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidently open.

Table 5. MAXIMUM RATINGS TABLE

Symbol	Pin	Rating	Value	Unit
VCTRL	1	$V_{CONTROL}$ pin	−0.3, $V_{ctrl,max}$(*)	V
CS/ZCD	3	CS/ZCD Pin	−0.3, +9	V
DRV	4	Driver Voltage Driver Current	−0.3, V_{DRV} (*) −500, +800	V mA
VCC	5	Power Supply Input	−0.3, + 30	V
VCC	5	Maximum (dV/dt) that can be applied to VCC	TBD upon test engineer measurements	V/s
FB	6	Feedback Pin	−0.3, +9	V
P_D $R_{\theta JA}$		Power Dissipation and Thermal Characteristics Maximum Power Dissipation @ T_A=70°C Thermal Resistance Junction to Air	 550 145	 mW °C/W
T_J		Operating Junction Temperature Range	−40 to+125	°C
$T_{J,max}$		Maximum Junction Temperature	150	°C
$T_{S,max}$		Storage Temperature Range	−65 to 150	°C
$T_{L,max}$		Lead Temperature (Soldering, 10 s)	300	°C
MSL		Moisture Sensitivity Level	1	−
		ESD Capability, HBM model (Note 1)	> 2000	V
		ESD Capability, Machine Model (Note 1)	> 200	V

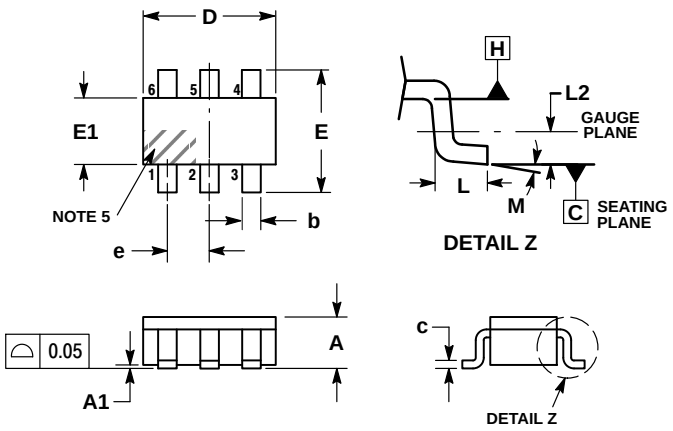
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

*"$V_{ctrl,max}$" is the VCTRL pin clamp voltage. "V_{DRV}" is the DRV clamp voltage ($V_{DRVhigh}$) if V_{CC} is higher than ($V_{DRVhigh}$). "V_{DRV}" is V_{CC} otherwise.

1. This device(s) contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per JEDEC Standard JESD22−A114E
   Machine Model Method 200 V per JEDEC Standard JESD22−A115−A
2. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE U

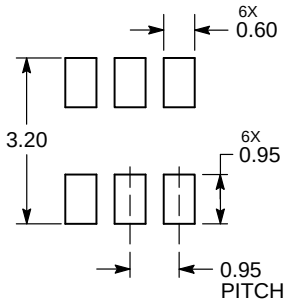


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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